

3rd MemoCIS Training School
'Memristors – Devices, Models, Circuits, Systems and Applications', Haifa, Israel, 7- 9.6.2017

PROGRAM

Day 1 Wednesday May 7, 2017

08:30 – 12:30 (EXUVLREUHDNIDVDGRSH□□JHYHZ□□H6HLGH□□RUNVRSVSHDNHUVBUH□)

09:30 – 13:30 5HJLVUD□□RDG□□HOERPH

13:30 – 14:30 Lunch Break

14:30 – 18:30 Onur Mutlu - "Memory Systems: Problems and Solution Directions"

19:30 – 21:00 Dinner



PROGRAM

Day 2 Thursday June 8, 2017

08:30 – 10:15 Pierre-Emmanuel Gaillardon - "Design Opportunities of Resistive Back-End Memories: From Technology to Reconfigurable Logic"

10:15 – 10:45 Morning Break

10:45 – 12:30 Shahar Kvatinsky - "mMPPU - memristive Processing Unit - a Real In-Memory Processing System"

12:30 – 15:00 Lunch Break + Trainee poster session

15:00 – 16:45 Joseph Friedman - "Spintronic Logic"

16:45 – 17:15 Coffee break

17:15 – 19:00 Massimiliano Di Ventra

19:00 – 21:00 Dinner & Social Event



PROGRAM

Day 3 Friday June 9, 2017

08:30 – 10:15 Alon Ascoli - "System theoretic methods for the analysis of memristor systems"

10:15 – 10:45 Morning Break

10:45 – 12:30 Ioannis Vourkas - "Logic Design and Computing Circuits with Memristors"

12:30 – 13:00 Closing remarks

